WHAT WE CLAIM IS:

1. A semiconductor integrated circuit device comprising:

a semiconductor substrate containing a first region and a second region;

first MISFETs formed in said first region;

second MISFETs formed in said second region, each of said second MISFETs having a gate electrode and impurity regions;

a first insulating layer formed over said first and second MISFETs;

word lines formed over said first region;

bit lines formed over said word lines and said first insulating layer,

wherein each of said first MISFETs is included in an individual one of plural memory cells, each of said memory cells being connected to one of said bit lines and one of said word lines;

a second insulating layer formed over said bit lines and first insulating layer,

wherein said first and second insulating layer having a hole formed therethrough;

a plug formed in said hole; and

a wiring layer formed over said second insulating film, said wiring layer being electrically connected to said impurity region via said plug.